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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	10/062,993	
			Filing Date	1/31/02 #14	
			First Named Inventor	Steven T. Ig, et al.	
			Group Art Unit	2825	
			Examiner Name	Kik, Phallaka	
Sheet	1	of	4	Attorney Docket Number	SPLX.P0100

U.S. PATENT DOCUMENTS						
Examiner's Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
PS	1.	5,521,835		05-28-1996	Trimberger	
PS	2.	5,610,829		03-11-1997	Trimberger	
PS	3.	6,035,107		03-07-2000	Kuehlman et al.	
PS	4.	6,216,252	B1	04-10-2001	Dangelo et al.	
PS	5.	6,334,205		12-25-2001	Iyer et al.	
PS	6.	6,470,478	B1	10-22-2002	Bargh et al.	
PS	7.	6,496,972	B1	12-17-2002	Segal	
PS	8.	6,523,156	B2	02-18-2003	Cint	
PS	9.	6,574,779	B2	06-03-2003	Allen et al.	

NON PATENT LITERATURE DOCUMENTS					
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	10.	Yi, J. H. et al., Technology Mapping for Storage Elements Based on BDD matching, Proceedings of the 40 th Midwest Symposium on Circuits and Systems, pp. 1099-1102, vol.2, August 1997.			

Examiner Signature	Phallaka Kik	Date Considered	5/1/2004
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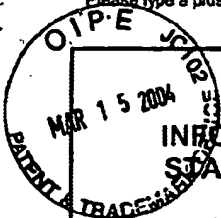
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Prior submitted on 03/31/03

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE



Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/062,993
		Filing Date	1/31/02
		First Named Inventor	Steven Teig, et al.
		Group Art Unit	2122 2825
		Examiner Name	P. KUK
Sheet	4 of 4	Attorney Docket Number	SPLX.P0100

RELATED U.S. PATENT APPLICATIONS

Examiner's Initials	Cite No. ¹	U.S. Patent Application Serial Number	Name of Patentee or Applicant of Cited Document	Date of Filing MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
<i>[initials]</i>	130	10/062,017	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	231	10/061,459	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	332	10/062,014	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	433	10/062,044	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	534	10/066,264	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	635	10/066,188	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	736	10/062,992	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	837	10/061,474	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	938	10/061,719	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	1039	10/066,456	Steven Teig & Asmus Hetzel	01-31-02	
<i>[initials]</i>	1140	10/062,047	Steven Teig & Asmus Hetzel	01-31-02	

U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
<i>[initials]</i>	412	5,649,165		Jain et al.	07-15-97	
<i>[initials]</i>	431	6,301,687	B1	Jain et al.	10-09-01	

Examiner Signature	<i>[Signature]</i>	Date Considered	5/1/2004
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<p>Substitute for form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p>(us as many sheets as necessary)</p>		Application Number	10/062,993		
		Filing Date	1/31/02		
		First Named Inventor	Steven T. Ig. et al.		
		Group Art Unit	2122-2825		
		Examiner Name	P. KVR		
Sheet	2	of	4	Attorney Docket Number	SPLX.P0100

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
<i>PK</i>	11	D. Jongeneel, R. Ollen, Y. Watanabe and R. K. Brayton, Area and Search Space Control for Technology Mapping, 37 th Design Automation Conference, 86-91, 2000.		
<i>PK</i>	12	Henrik Reif Andersen, An Introduction to Binary Decision Diagrams, October 1997 (minor revisions April 1998), 36 pp.		
<i>PK</i>	13	Jerry Burch and David Long, Efficient Boolean Function Matching, Proc. ICCAD 1992, 408-411.		
<i>PK</i>	14	John Fishburn, A Depth-Decreasing Heuristic for Combinational Logic; or How to Convert Ripple-Carry Adder into a Carry-Lookahead Adder or Anything In-Between, Proceedings of the 27 th Design Automation Conference, 361-364, 1990.		
<i>PK</i>	15	Kamal Chaudhary and Massoud Pedram, A Near Optimal Algorithm for Technology Mapping Minimizing Area under Delay Constraints, Proceedings of the 29 th Design Automation Conference, 492-498, 1992.		
<i>PK</i>	16	Kurt Keutzer, DAGON: Technology Binding and Local Optimization by DAG Matching, Proceedings of the 24 th Design Automation Conference, 341-347, 1987.		
<i>PK</i>	17	Randal Bryant, Symbolic Boolean Manipulation with Ordered Binary Decision Diagrams, CMU CS Tech Report CMU-CS-92-160.		
<i>PK</i>	18	Uwe Hinsberger and Reiner Kolla, Boolean Matching for Large Libraries, Proceedings of the 35 th Design Automation Conference, 206-211, June 1998.		
<i>PK</i>	19	Yuji Kukimoto, Robert K. Brayton, and Prashant Sawkar, Delay-Optimal Technology Mapping by DAG Covering, Dept. of Electrical Engineering and Computer Science, University of California, Berkeley, Strategic CAD Laboratories, Intel Corp., October 1997.		
<i>PK</i>	20	Zbigniew J. Czech, et al., An Optimal Algorithm for Generating Minimal Perfect Hashing Functions, Information Processing Letters, 43(5): 257-264, October 1992		

Examiner Signature	<i>Phillip K. V. R.</i>	Date Considered	5/1/04
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Prior submitted

12/01/03

B. on PTO/SB/08 a & b (05-03)

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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

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Sheet

3

of

4

Application Number

10/062,993

Filing Date

1/31/02

First Named Inventor

Steven T. Ig, et al.

Group Art Unit

2122-2825

Examiner Name

P. KIK

Attorney Docket Number

SPLX.P0100

U.S. PATENT DOCUMENTS

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<i>PK</i>	21	5,519,630		05-21-1996	Nishiyama et al.	
<i>PK</i>	22	5,537,341		07-16-1996	Rose et al.	
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<i>PK</i>	24	5,574,441		05-19-1998	Tokunoh et al.	
<i>PK</i>	25	5,787,010		07-28-1998	Schaefer et al.	
<i>PK</i>	26	6,023,566		02-08-2000	Belkhale et al.	
<i>PK</i>	27	6,301,696	B1	11-09-2001	Lien et al.	

NON PATENT LITERATURE DOCUMENTS

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<i>PK</i>	28	Crastes, M. et al., A Technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.	
<i>PK</i>	29	Devadas, S. et al., Synthesis and Optimization for robustly delay-fault testable combinational logic circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp. 221-227.	

Examiner
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Considered

5/1/2004

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